Patent Claims

1. Line driver arrangement (1) for driving signals (Vi, Vo) via at least one subscriber line (4), having:

an input (2) for injecting an input signal (Vi) and having an output (3) at which a signal (Vo) which is to be driven via the subscriber line (4) can be tapped off,

a digital amplifier (6) which produces a pulse-width-modulated signal (Vd, id) on the output side from the input signal (Vi) or from a signal (Vs) derived from it,

an analog amplifier (5), which produces an analog signal (Ve', ia) on the output side from the input signal (Vi) or from a signal derived from it,

with the outputs of the amplifiers (5, 6) being coupled such that the signal (Vo) to be driven results from superimposition of the analog signal (Ve', ia) and the digital signal (Vd, id),

with the gain of the analog amplifier (5) being matched to the gain of the digital amplifier (6) such that scatter and/or overshoot on the digital signal (Vd, id) are at least reduced after the superimposition.

2. Line driver arrangement according to Claim 1, characterized
in that a feedback path (16) is provided, via which the signal (Vo, io) which results from the superimposition of the analog and digital signals (Ve', ia; Vd, id) can be fed back with negative feedback to the input of the analog amplifier (5).

3. Line driver arrangement according to one of the preceding claims,
characterized
in that the analog amplifier (5) is arranged in an analog path (10), and the digital amplifier (6) is arranged in a digital path (11), with the two paths (10, 11) being arranged in parallel with one another.

4. Line driver arrangement according to Claim 3,
characterized
in that a filter (12), in particular a low-pass filter, is provided, follows the digital amplifier (6) in the digital path (11) and carries out frequency smoothing as well as filtering of the digital signal (Vd).

5. Line driver arrangement according to one of Claims 3 or 4,
characterized
in that a matching circuit (14) is provided, is connected upstream of the analog amplifier (5) in the analog path (10) and carries out phase matching and/or amplitude matching of the input signal (Vi) to the output signal (Vo).

6. Line driver arrangement according to one of the preceding claims,
characterized
in that the analog amplifier (5) is followed by a resistance network (40), at whose output an analog current (ia) can be tapped off, and in that a potential (Vs) which is tapped off from the resistance network (40) can be injected into the digital amplifier (6), which uses this to produce on the output side a digital current (id) which is superimposed on the analog current (ia).

7. Line driver arrangement according to Claim 6,
characterized

in that the resistance network (40) has at least one measurement resistance (44) via which the analog current (ia) is passed, and has a voltage divider (45) across which the potential (Vs) which is injected into the digital amplifier (6) can be tapped off.

8. Line driver arrangement according to Claim 7, characterized
in that the resistance value of the measurement resistance (44) is very much less than the resistance values of the voltage divider resistances (45).

9. Line driver arrangement according to one of the preceding claims,
characterized
in that at least one transformer (13, 15) is provided at the output (3) of the line driver (1).

10. Line driver arrangement according to one of the preceding claims,
characterized
in that a load which is in the form of a transformer (13) is provided at the output (3) of the power driver arrangement (1).

11. Line driver arrangement according to one of Claims 9 or 10,
characterized
in that the transformer (13) is designed such that its bandwidth matches the bandwidth of the signal (Vi, Vo) to be driven.

12. Line driver arrangement according to one of Claims 9 to 11,
characterized
in that at least one transformer (13) has a very high transformation ratio in the region of at least 1:4, in

particular in the region of more than 1:6, between the primary and the secondary sides.

13. Line driver arrangement according to one of the preceding claims,
characterized
in that a further transformer (15) is provided, is arranged in the analog path (10), and follows the analog amplifier (5).

14. Line driver arrangement according to Claim 13,
characterized
in that the further transformer (15) has a lower transformation ratio than the first transformer (13), in particular a transformation ratio of about 1:1.

15. Line driver arrangement according to one of the preceding claims,
characterized
in that a divider (18) is provided in the feedback path (16), and has a feedback factor (f) by which the fed-back signal is divided.

16. Line driver arrangement according to Claim 15,
characterized
in that the feedback factor (f) corresponds to the transformation ratio of the transformer which follows the digital amplifier (6).

17. Line driver arrangement according to one of the preceding claims,
characterized
in that the power driver arrangement (1) has a further feedback device (28) which feeds back the output signal (Vo) with positive feedback to the input (2), with the elements of the control loop which results from this being designed such that the impedance of the power driver arrangement (1) is variable.

18. Line driver arrangement according to Claim 17, characterized
in that [lacuna] for the variable impedance has a synthesis factor (m) which is proportional to the ratio of the load (26) to an output resistance (25).

19. Line driver arrangement according to one of the preceding claims, characterized in that a control device (8) is provided for controlling the amplifiers (5, 6).

20. Line driver arrangement according to one of the preceding claims,
characterized
in that the analog amplifier (5) is in the form of an inverting amplifier.

21. Line driver arrangement according to one of the preceding claims,
characterized
in that the digital amplifier (6) has a comparator (30, 50) which is coupled to the input of the digital amplifier (6) and is followed, as the output stage (31, 32; 51, 52), by a power inverter.

22. Line driver arrangement according to one of the preceding claims,
characterized
in that the digital amplifier (6) has a PWM characteristic, such that its digital output signals (Vd, id) are pulse-width modulated.

23. Line driver arrangement according to one of the preceding claims,
characterized
in that the line driver arrangement (1) is in the form of an ADSL driver circuit.

24. Line driver arrangement according to one of the preceding claims,
characterized
in that circuit means are provided, by means of which the switching frequency is matched to the amplitude of the output signal.

25. Line driver arrangement according to one of the preceding claims,
characterized
in that the signals (Vi, Vo) to be driven are speech signals and/or data signals.

26. Line driver arrangement according to one of the preceding claims,
characterized
in that the line driver arrangement (1) is completely differential.